IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket Number 15483US02

In re Application of:	)	
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Ramadas Lakshmikanth Pai	)	**ELECTRONICALLY FILED**
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Serial No.: 10/816,118	)	**February 7, 2011**
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Filing Date: 4/1/2004	)	
	)	
Examiner: Anner N. Holder	)	
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Confirmation No.: 8484	)	
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Art Unit No. 2483	)	
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REPLY BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This reply brief is filed in response to Examiner's Answer of December 6, 2010.

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I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation having a place of business at 5300 California Drive, Irvine California 92617, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefrom.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-3, 5, 7-9 and 15 are rejected under 35 U.S.C. 103(a) as anticipated by U.S. Patent 6,310,921 to Yoshioka ("Yoshioka") in view of U.S. Patent 5,706,059 ("Ran").

Claims 4, 6, and 10-14 are cancelled without prejudice.

Claims 1-3, 5, 7-9, and 15 are appealed.

IV. STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a video request manager comprising:

a first state machine (Specification at 14, Lines 14-15, Figure 4, 405R) for commanding a memory controller

(Figure 4, 309) to fetch reference pixels for a first portion of a picture; and

a second state machine (Specification at 14, Lines 14-15, Figure 4, 405W) for commanding a memory controller (Figure 4, 309) to write a second portion of the picture, wherein the second state machine loads the memory controller with the second portion while the memory controller fetches the reference pixels (Specification at 14, line 31 - p. 15, line 3).

Claim 5 is directed to a circuit for decoding video data, said circuit comprising:

a motion vector address computer (Specification at 13, lines 23-28, Figure 3, 308) for calculating at least one address for reference pixels for a first portion of a picture;

a motion compensator (Specification at 14, lines 23-27, Figure 4, motion compensator 312)for decoding another portion of the picture;

a video request manager (Specification at 14, lines 10-11, Figure 4, 310) comprising:

a first state machine (Specification at 14, lines 14-15, Figure 4, 405R) for issuing a command to fetch reference pixels for a first portion of a picture (Specification at 14, lines 28-30); and

a second state machine (Specification at 14, lines 14-15, Figure 4, 405W) for issuing a command to write a second portion of the picture (Specification at 14, lines 28-30);

a memory controller (Figure 4, memory controller 309) for fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command, and wherein the memory controller loads the second portion of the picture while fetching the reference pixels.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 5, 7-9, and 15 as obvious from Yoshioka in view of Ran.

VII. ARGUMENT: CLAIMS 1

Claim 1 is recited below:

> A video request manager comprising:
>
> a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; and
>
> a second state machine for commanding a memory controller to write a second portion of the picture, wherein the second state machine loads the memory controller with the second portion while the memory controller fetches the reference pixels.

Claim 1 was rejected under 35 U.S.C. 103(a) as being obvious from the combination of Yoshioka and Ran. In the Appeal Brief, Section VII, Appellant argued that the rejection to claim 1 should be reversed because the combination of Yoshioka and Ran does not teach "fetching reference pixels for a first portion of a picture" and "load the memory controller of a picture while the memory controller fetches the reference pixels" and because Yoshioka and Ran cannot be combined in the manner suggested in the Office Action.

A. THE REJECTION TO CLAIM 1 SHOULD BE REVERSED BECAUSE THE COMBINATION OF YOSHIOKA AND RAN DOES NOT TEACH "FETCHING REFERENCE PIXELS FOR A FIRST PORTION OF A PICTURE" AND "LOADS THE MEMORY CONTROLLER WITH THE SECOND PORTION WHILE THE MEMORY CONTROLLER FETCHES THE REFERENCE PIXELS".

In Examiner's Answer at 7, Examiner argues that:

> pixel read/write extract the rectangular local serach area not entire frame or poicture when performing motion

compensation. The local search area retrieved a is a portion of the current frame. [col. 11, line 64-col. 12, line 7; col. 13, line 56 - col. 14, line 4; col. 14 lines 38-45; col. 18, lines 6-27]….

Assignee respectfully submits that the foregoing is incorrect and also fails to establish "fetching reference pixels for a first portion of a picture" and "loads the memory controller with the second portion while the memory controller fetches the reference pixels".

It is first noted pixels fetched during motion compensation are from a *different* frame or pocture. ISO13818-2 defines motion compensation "The use of motion vectors to improve the efficiency of the prediction of sample values. The prediction uses motion vectors to provide offsets into the past and/or future reference frames or reference fields containing previously decoded sample values that are used to form the prediction error. Clearly a past or future reference frame would not be the current frame as alleged by Examiner.

Additionally, Examiner argues, Examiner's Answer at 7:

Ran discloses motion estimation device which writes to a memory while (i.e., simultaneously) reading from another part of he memory [Abstract; col. 3, lines 4-10]. Ran retrieves search data from the other two ports of the memory that is equivalent to a read operation. The loading of a portion of memory as disclosed by Ran is equivalent to a writing operation.

Appellant respectfully disagrees. Ran teaches, col. 3, lines 4-10 that "The second memory is divided into three parts. The size of the parts of the second memory are such that two of the parts contain a current search window used by the processing elements, and a third of the parts is loaded with pixel values for a next search window while the

processing elements perform a search on the current search window."

First, in the foregoing context, "that the third of the parts is loaded with pixel values … while the processing elements perform a search…", it is not clear when the foregoing is written. In the foregoing context, "is loaded" merely means that the third of the parts stores the "pixels values for a next search window" while …. It is quite possible that the foregoing could have been written prior to when "the processing elements perform a search on the current search window."

Secondly, "loaded with pixel values for a next search window while the processing elements perform a search on the current search window", likely means that a time period defined from the beginning of when a processing element performs a search and ending when a processing element performs a search overlaps a time when "the third part is loaded". Thus, it is not necessarily the case that retrieval by the processing elements occurs simultaneously as loading the third part.

B. THE REJECTION OF CLAIM 1 SHOULD BE REVERSED BECAUSE IT WOULD NOT BE OBVIOUS TO MODIFY YOSHIOKA WITH THE TEACHINGS OF RAN

Finally, even Yoshioka was deemed to teach "fetch reference pixels for a first portion of a picture" and "write a second portion of the picture", Assignee still maintains traverse. Although the Office Action indicates that "It is well known in the art that memory is capable of performing simultaneous read/write operations…" Office Action at 2-3, it would not be possible to apply to Yoshioka. Note that Yoshioka, "extracts a rectangle area

indicated by the motion vector" and that "The decode result given by the pixel read/write unit 11 here is stored in the external memory 3 via the memory controller 6."

However, even in view of the teachings of Ran, Yoshioka could not be modified to perform the foregoing simultaneously, because "the decode result … stored in the external memory 3", only becomes available when "the rectangle area" is blended with the block. Thus, the rectangle area has to be extracted before the decode result can be stored in the external memory 3. Accordingly, Assignee respectfully traverses that it "would have been obvious … to incorporate the simultaneous read/search and write teaching of Ran with the device of Yoshioka".

In response, Examiner has argued that Yoshioka and Ran are in the same field of endeavor, and that "the test for obviousness is not whether the features of a second reference may be bodily incorporated into the structure of the primary reference… See In re Keller". Answer at 8.

First, it is well settled law that the mere fact that two references are in the same field of endeavor is not conclusive proof of obviousness to combine. As noted in MPEP 2141:

> Office personnel should consider all rebuttal evidence that is timely presented by the applicants when reevaluating any obviousness determination. Rebuttal evidence may include evidence of "secondary considerations," such as "commercial success, long felt but unsolved needs, [and] failure of others"(*Graham v. John Deere Co.*, 383 U.S. at 17, 148 USPQ at 467), and may also include evidence of unexpected results. As set forth above, Office personnel must articulate findings of fact that support the rationale relied upon in an obviousness rejection. As a result, applicants are likely to

submit evidence to rebut the fact finding made by Office personnel. For example, in the case of a claim to a combination, applicants may submit evidence or argument to demonstrate that:

(A) one of ordinary skill in the art could not have combined the claimed elements by known methods (e.g., due to technological difficulties);

(B) the elements in combination do not merely perform the function that each element performs separately; or

(C) the results of the claimed combination were unexpected.

Once the applicant has presented rebuttal evidence, Office personnel should reconsider any initial obviousness determination in view of the entire record. See e.g., *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); *In re Eli Lilly & Co.*, 90 F.2d 943, 945, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990). All the rejections of record and proposed rejections and their bases should be reviewed to confirm their continued viability."

In the present case, Appellant presents evidence that the fetching and writing cannot be combined to be performed simultaneously because in the proposed combination, the data that is to be written is data dependent on the data that is to be fetched. Examiner has not considered this rebuttal evidence.

Moreover, Keller held that "To justify combining reference teachings in support of a rejection it is not necessary that a device shown in one reference can be physically inserted into the device shown in in the other. *In re Griver, 53 CCPA 815, 354 F.2d 377, 148 USPQ 197 (1966); In re Billingsley, 47 CCPA 1108, 279 F.2d 689, 126 USPQ 370 (1960).*"

The foregoing cases merely dealt with circumstances wherein a mechanical element of a secondary reference was not made to fit into a mechanical element of the primary reference. The courts reasoned that although the former could not fit into the latter, the former or the latter could easily be adapted to fit ("Naturally the shape of the groove would be adapted to that of the rib in which it is located." *In re Griver)*. The foregoing are entirely distinguishable from the present case.

Keller, and it predecessor's noted, e.g., that "the shape of the groove would be adapted to that of the rib in which it is located". However, the problem presented in this case, that the fetching and writing cannot be performed simultaneously because in the proposed combination, the data that is to be written is data dependent on the data that is to be fetched, is, if not impossible, far more complex than the problem in Keller.

Accordingly, Appellant respectfully requests that the rejection to claim 1 and its dependents be REVERSED.

VIII. ARGUMENT: CLAIMS 5

Claim 5 is copied below:

> 5. (Currently Amended) A circuit for decoding video data, said circuit comprising:
>
> a motion vector address computer for calculating at least one address for reference pixels for a first portion of a picture;
>
> a motion compensator for decoding another portion of the picture;
>
> a video request manager comprising:
>
> a first state machine for issuing a command to fetch reference pixels for a first portion of a picture; and
>
> a second state machine for issuing a command to write a second portion of the picture;
>
> a memory controller for fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command, and wherein the memory controller loads the second portion of the picture while fetching the reference pixels.

Claim 5 was rejected under 35 U.S.C. 103(a) as being obvious from the combination of Yoshioka and Ran. Appellant hereby incorporates Section VII by reference and submits that the rejection to claim 5 and its dependents should be REVERSED for the reasons stated therein.

CONCLUSION

For the foregoing reasons, claims 1-18 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: February 7, 2011

Respectfully submitted,

/Mirut Dalal/

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CLAIMS APPENDIX

1. A video request manager comprising:

a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; and

a second state machine for commanding a memory controller to write a second portion of the picture, wherein the second state machine loads the memory controller with the second portion while the memory controller fetches the reference pixels.

2. The video request manager of claim 1, wherein the second state machine commands the memory controller to write the second portion, such that a resource contention occurs between the command to fetch reference pixels, and the command to write the second portion.

3. The video request manager of claim 2, wherein the second state machine commands the memory controller to write the second portion, such that the command to fetch reference pixels is given priority during the resource contention.

4. (Cancelled).

5. A circuit for decoding video data, said circuit comprising:

a motion vector address computer for calculating at least one address for reference pixels for a first portion of a picture;

a motion compensator for decoding another portion of the picture;

a video request manager comprising:

a first state machine for issuing a command to fetch reference pixels for a first portion of a picture; and

a second state machine for issuing a command to write a second portion of the picture;

a memory controller for fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command, and wherein the memory controller loads the second portion of the picture while fetching the reference pixels.

6. (Cancelled).

7. (Previously Presented) The circuit of claim 5, wherein the memory controller further comprises:

an arbiter for causing the memory controller to give priority to the command to fetch the reference pixels.

8. (Previously Presented) The circuit of claim 5, wherein the memory controller further comprises:

a write buffer for storing the second portion of the picture while fetching the reference pixels.

9. (Original) The circuit of claim 8, wherein the memory controller writes the second portion of the picture from the write buffer to a memory system, after fetching the reference pixels.

10-14. (Cancelled).

15. (Previously Presented) The video request manager of claim 1, wherein the second state machine loads the memory controller with the second portion reconstructed from decoding while the memory controller fetches the reference pixels.

EVIDENCE APPENDIX

There are no pages in this appendix

RELATED PROCEEDINGS APPENDIX

There are no pages in this Appendix.